

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
26 May 2005 (26.05.2005)

PCT

(10) International Publication Number  
**WO 2005/048115 A3**

(51) International Patent Classification<sup>7</sup>: **G06F 13/16**

(21) International Application Number:  
PCT/IB2004/052281

(22) International Filing Date:  
3 November 2004 (03.11.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
03104176.7 13 November 2003 (13.11.2003) EP

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

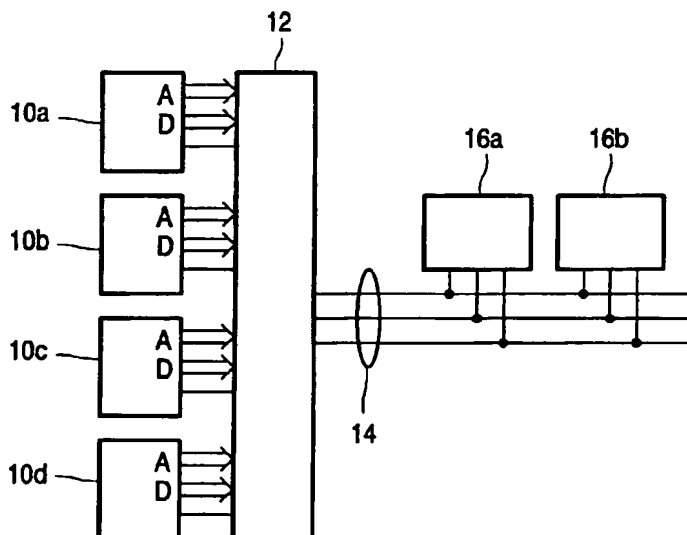
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Declaration under Rule 4.17:**

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ,

[Continued on next page]

(54) Title: **ELECTRONIC DATA PROCESSING CIRCUIT THAT TRANSMITS PACKED WORDS VIA A BUS**



(57) Abstract: An electronic data processing circuit contains a plurality of data handling units (10a-d, 16a-b) with data outputs, at least part of the data handling units having address outputs. The data handling units supply words of preferably selectable size to a bus. A bus controller (20) is arranged to control access to the bus in successive access cycles. The bus controller (20) causes data bits from a plurality of data words from respective ones of the data handling units (10a-d, 16a-b), to be placed in combination on the data lines in a same bus cycle. The bus controller causes write addresses that the respective ones of the data handling units (10a-d, 16a-b) supply for respective ones of the plurality of data words to be placed on the address lines in a plurality of respective bus cycles. Preferably, the temporal or spatial arrangement of the data words on the bus lines is adapted so as to minimize the number of logic level changes on the bus.



BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

(88) Date of publication of the international search report:  
14 July 2005

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

**Published:**

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments